

MS-7233

Version 0A
08/09/2005 Update

CPU:

Intel LGA775 Processor

System Chipset:

SIS 656 + SiS 965L

On Board Chipset:

LPC Super I/O -- W83697HF
LAN PHY -- VT6103
IEEE1394 -- VT6307
AC97 CODEC -- RealTek ALC850

CLOCK Chip :

ICS953401+ Buffer ICS9P932

Main Memory:

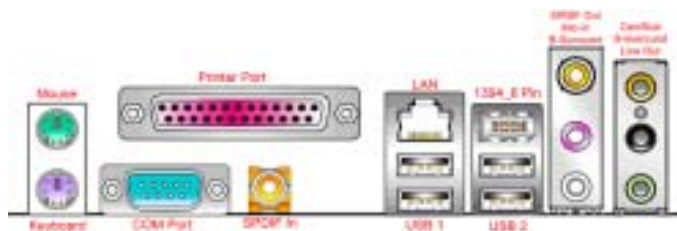
DDR2 DIMM Slot *4

Expansion Slots:

PCI EXPRESS x16 Slot *1
PCI EXPRESS x1 Slot *1
PCI2.2 Slot *2

PWM:

INTERSIL ISL6565ACV



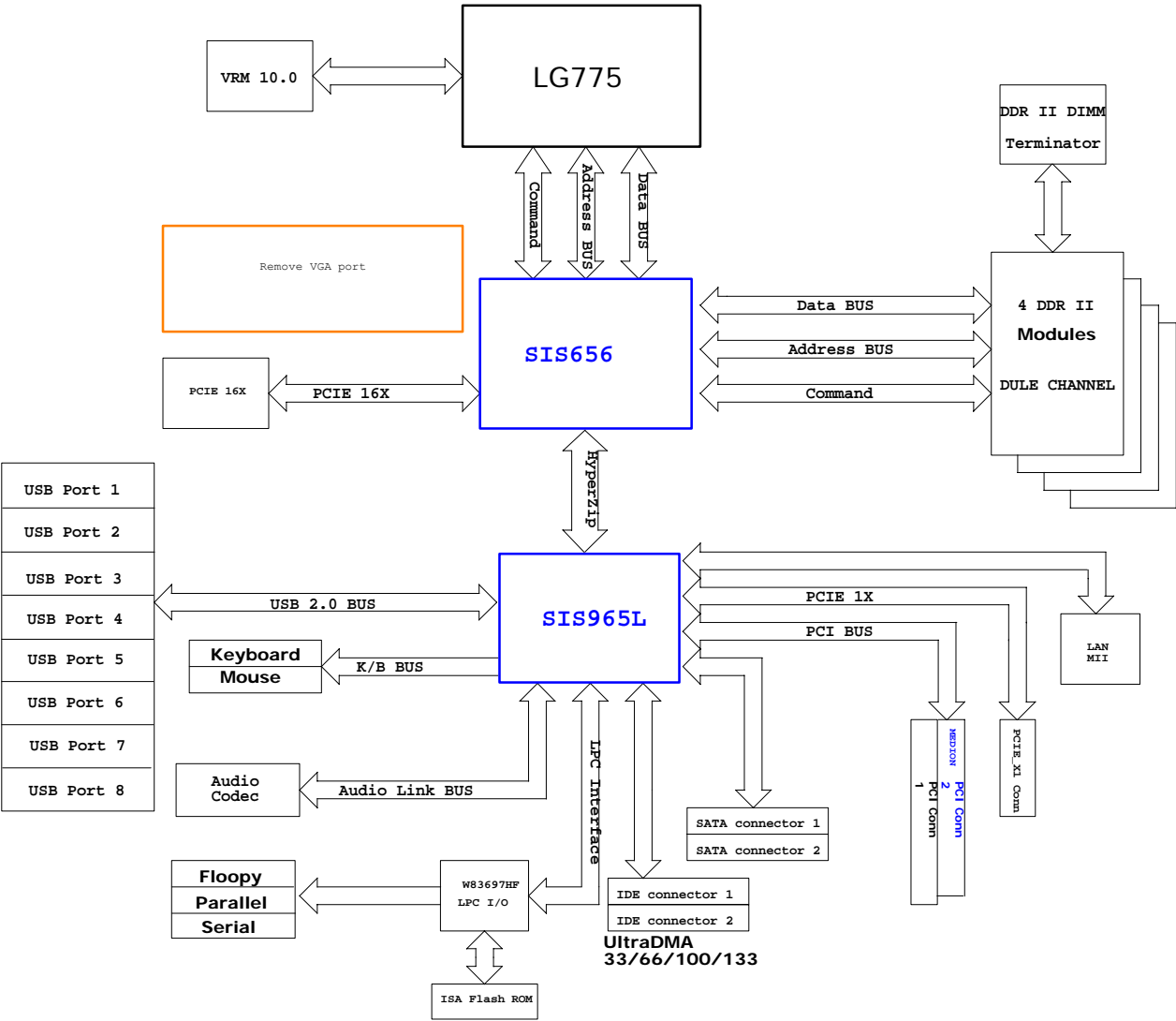
Title	Page
Cover Sheet	1
Block Diagram	2
Power Generation	3
Intel LGA775	4-6
NB SIS 656FX	7-11
DDR Slot & Termination	12-15
SB SIS 965L	16-19
PCI Express_X16,X1	20
PCI slot 1 & 2	21
IDE ATA 66/100 Connectors	22
USB CONNECTORS	23
Clock Synthesizer	24
Clock Buffer	25
AC97 S/W Audio	26
LPC83697HF/ROM	27
1394-VIA VT-6307	28
VT6103 LAN PYH	29
LPT & COM Port & K/M	30
VRM10.1 Intersil6565	31
ACPI POWER CONTROLLER (MS-7)	32
FAN	33
Front Panel&Power OK Circuit	34
OPTION PARTS	35
History	36

PCI Routing

PCI 2	INTC# IDSEL=AD23 MASTER=PREQ#1 PGNT#1 CPICLK4 INTB# IDSEL=AD21 MASTER=PREQ#3 PGNT#3 PCICLK3 INTA# IDSEL=AD20 MASTER=PREQ#5 PGNT#5 PCICLK0
PCI 3	INTD# IDSEL=AD19 MASTER=PREQ#2 PGNT#2 PCICLK2
1394	INTC# IDSEL=AD22 MASTER=PREQ#4 PGNT#4 1394PCLK

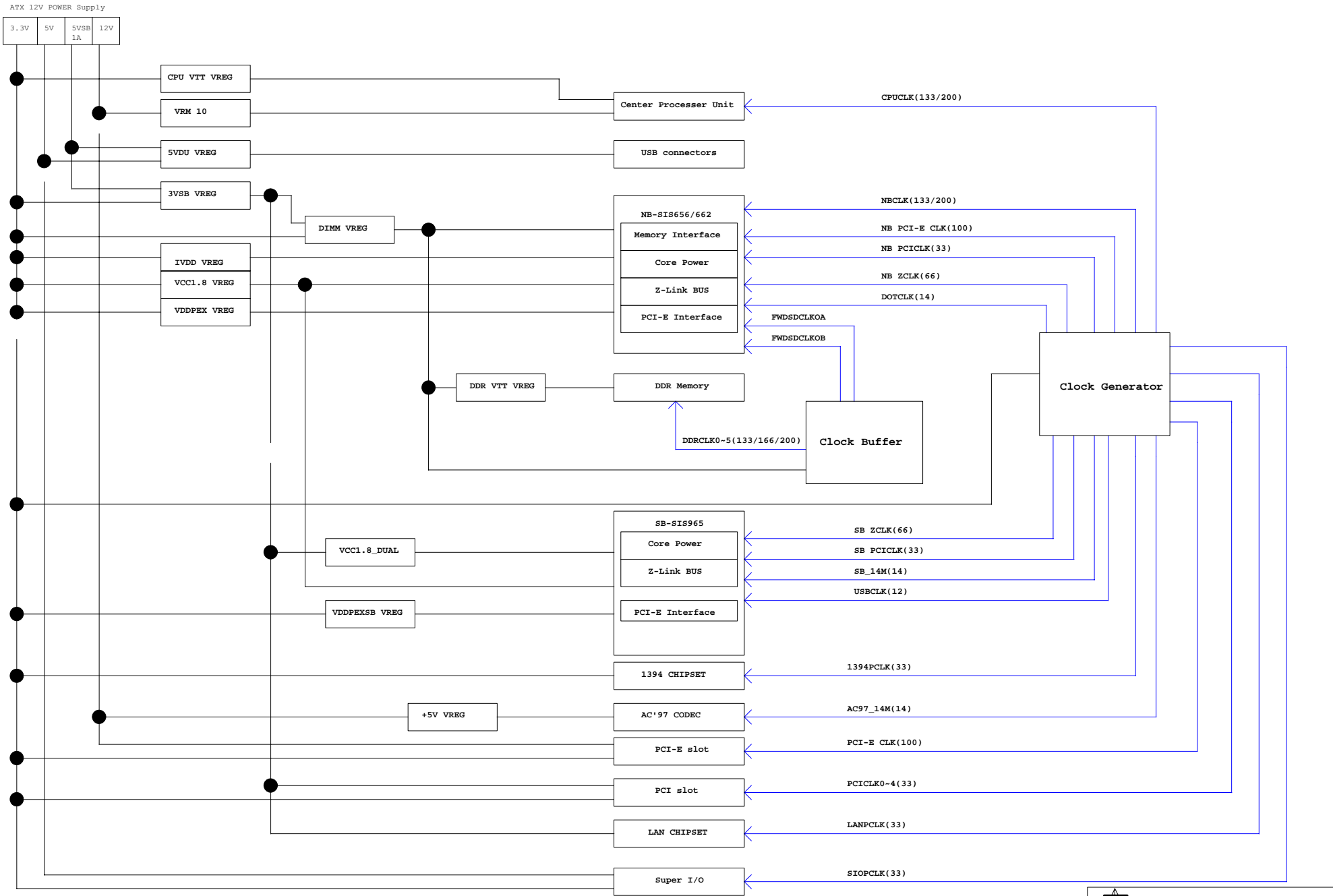
Block Diagram

MS-7114 Ver:2.0

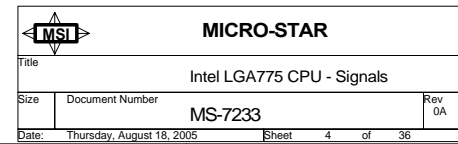


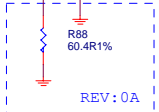
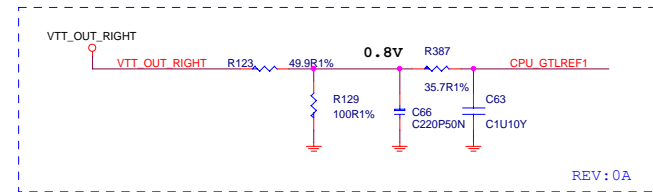
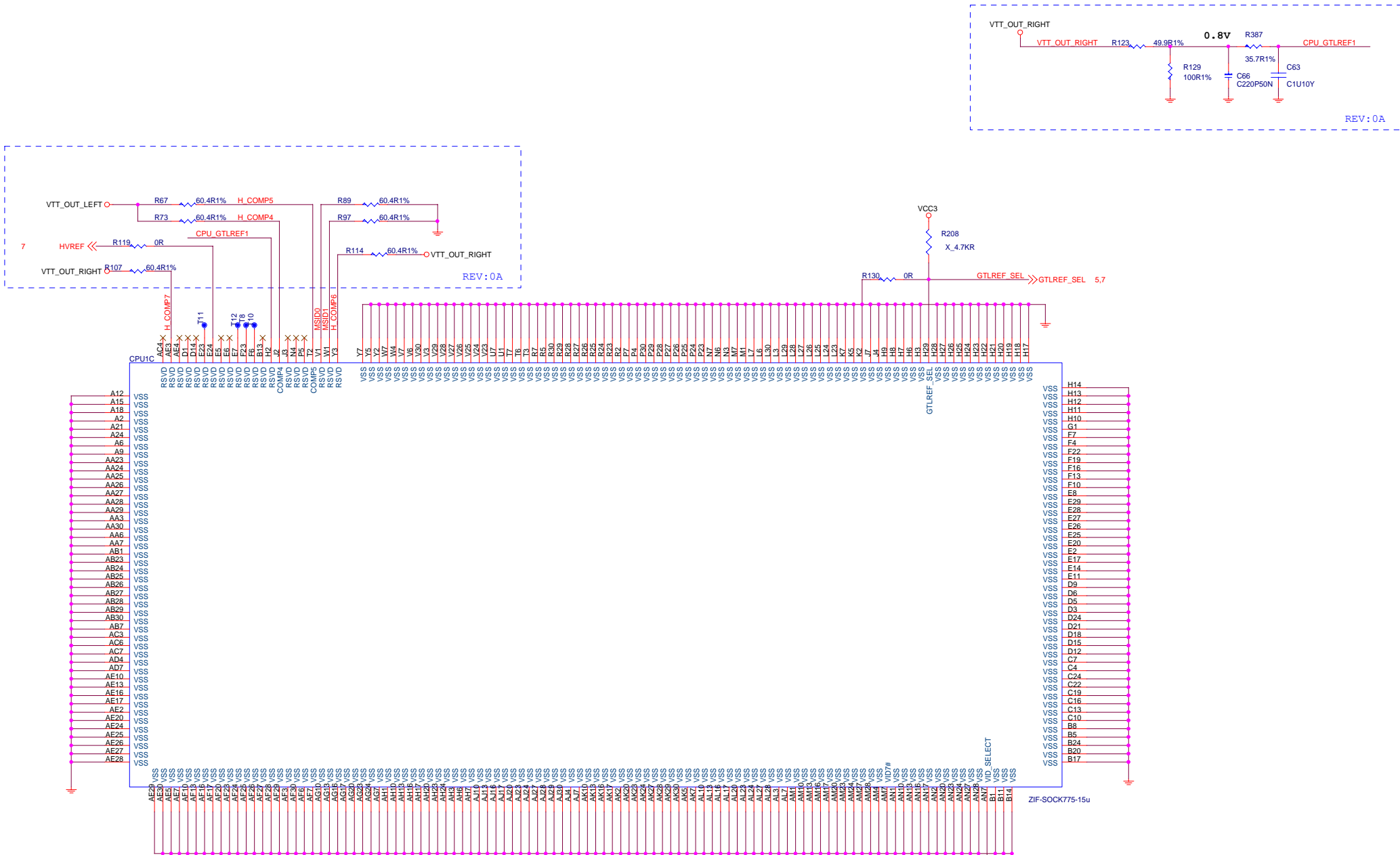
Power Delivery Map


CLOCK Delivery Map



REV: 0A





**MICRO-STAR**

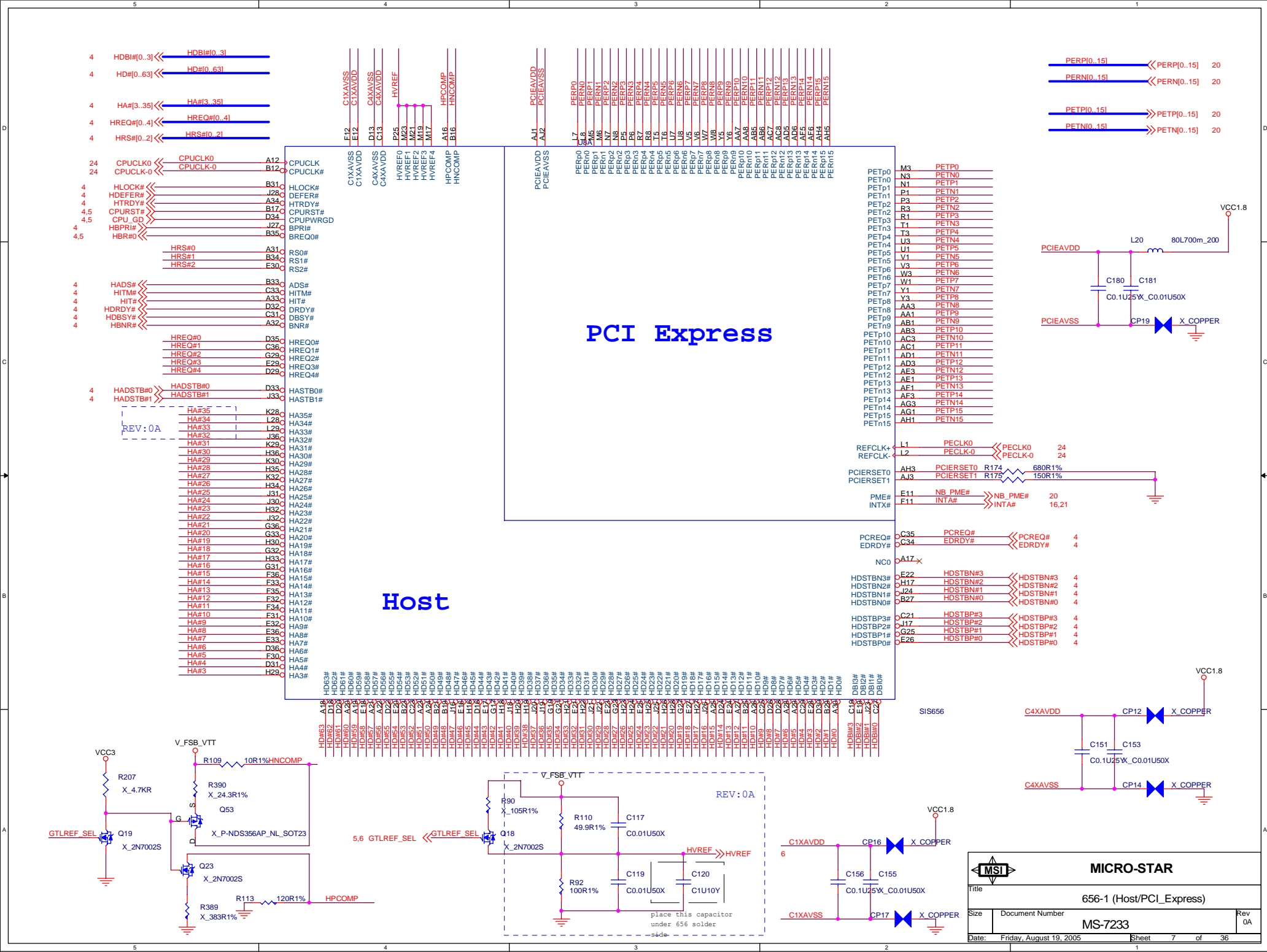
TitleIntel LGA775 CPU - GND

SizeDocument Number

MS-7233

Rev0A

Date: Friday, August 19, 2005Sheet6 of 36



MDA[0..63] << MDA[0..63] 12
DQMA[0..7] << DQMA[0..7] 12
DQSA[0..7] << DQSA[0..7] 12
DQSA#[0..7] << DQSA#[0..7] 12
MAA[0..17] << MAA[0..17] 12,14
CSA[0..3] << CSA[0..3] 12,14
ODTA[0..3] << ODTA[0..3] 12,14

MDA0 M34 MD0A
MDA1 N36 MD1A
MDA2 R36 MD2A
MDA3 R33 MD3A
MDA4 M36 MD4A
MDA5 P36 MD5A
MDA6 P35 MD6A
MDA7 P34 MD7A
DQMA0 N33 DQM0A
DQSA0 P36 DQS0A
DQSA#0 N32 DQS0A#
MDA8 T35 MD8A
MDA9 T34 MD9A
MDA10 V34 MD10A
MDA11 W36 MD11A
MDA12 R32 MD12A
MDA13 T36 MD13A
MDA14 V36 MD14A
MDA15 V35 MD15A
DQMA1 U36 DQM1A
DQSA1 U32 DQS1A
DQSA#1 U33 DQS1A#
MDA16 Y36 MD16A
MDA17 Y35 MD17A
MDA18 AB35 MD18A
MDA19 AB34 MD19A
MDA20 W33 MD20A
MDA21 W32 MD21A
MDA22 A32 MD22A
MDA23 AB36 MD23A
DQMA2 Y34 DQM2A
DQSA2 AA33 DQS2A
DQSA#2 AA36 DQS2A#
MDA24 AH30 MD24A
MDA25 AJ32 MD25A
MDA26 AM30 MD26A
MDA27 AN30 MD27A
MDA28 AG29 MD28A
MDA29 AH32 MD29A
MDA30 AM32 MD30A
MDA31 AN32 MD31A
DQMA3 AJ30 DQM3A
DQSA3 AL32 DQS3A
DQSA#3 AK32 DQS3A#
MDA32 AH24 MD32A
MDA33 AH23 MD33A
MDA34 AH21 MD34A
MDA35 AM20 MD35A
MDA36 AJ24 MD36A
MDA37 AJ23 MD37A
MDA38 AJ21 MD38A
MDA39 AH22 MD39A
DQMA4 AJ22 DQM4A
DQSA4 AJ22 DQS4A
DQSA#4 AK22 DQS4A#
MDA40 AM19 MD40A
MDA41 AT18 MD41A
MDA42 AT16 MD42A
MDA43 AR16 MD43A
MDA44 AT19 MD44A
MDA45 AN19 MD45A
MDA46 AN17 MD46A
MDA47 AM17 MD47A
DQMA5 AR18 DQM5A
DQSA5 AT17 DQS5A
DQSA#5 AP18 DQS5A#
MDA48 AN15 MD48A
MDA49 AM15 MD49A
MDA50 AM13 MD50A
MDA51 AT12 MD51A
MDA52 AP16 MD52A
MDA53 AT13 MD53A
MDA54 AN13 MD54A
MDA55 AN13 MD55A
DQMA6 AT14 DQM6A
DQSA6 AP14 DQS6A
DQSA#6 AR14 DQS6A#
MDA56 AT11 MD56A
MDA57 AN11 MD57A
MDA58 AR9 MD58A
MDA59 AP9 MD59A
MDA60 AR12 MD60A
MDA61 AP12 MD61A
MDA62 AP10 MD62A
MDA63 AT9 MD63A
DQMA7 AM11 DQM7A
DQSA7 AR10 DQS7A
DQSA#7 AT10 DQS7A#

U8B
MA0A AP33 MAA0
MA1A AN33 MAA1
MA2A AT34 MAA2
MA3A AR34 MAA3
MA4A AR35 MAA4
MA5A AP34 MAA5
MA6A AP35 MAA6
MA7A AM33 MAA7
MA8A AP36 MAA8
MA9A AN36 MAA9
MA10A AT33 MAA10
MA11A AR32 MAA11
MA12A AP32 MAA12
MA13A AM35 MAA13
MA14A AN34 MAA14
MA15A AM34 MAA15
MA16A AM29 MAA16
MA17A AM36 MAA17
RASA# AT32 RASA-
CASA# AP30 CASA-
WEA# AT31 WEA-

FWSDCLKOB K36 R FWSDCLKOB R333
FWSDCLKOB# K35 R FWSDCLKOB- R334
FWSDCLKOA K34 R FWSDCLKOA R332
FWSDCLKOA# L36 R FWSDCLKOA- R335

CS0A# AM31 CSA-0
CS1A# AN29 CSA-1
CS2A# AN31 CSA-2
CS3A# AT29 CSA-3
ODT0A AR30 ODTA0
ODT1A AP28 ODTA1
ODT2A AT30 ODTA2
ODT3A AR28 ODTA3
GCKE AJ33

ECCD0A/CKE0A AH34 CKEA0
ECCD1A/CKE1A AJ36 CKEA1
AL34 CKEA2
ECCD2A/CKE2A AL33 CKEA3
ECCD3A/CKE3A AH36
ECCD4A AH35
ECCD5A AK34
ECCD6A AL36
ECCD7A AJ34
ECCDQMA AK35
ECCDQSA AK36
ECCDQSA# AK36

D1XAVDD A13 D1XAVDD
D1XAVSS B13 D1XAVSS
D4XAVDD AH28 D4XAVDD
D4XAVSS AJ28 D4XAVSS

DDRVREF0 AE19
DDRVREF1 AE23
DDRVREF2 AC25
DDRVREF3 V25

DDRCOMP AJ29
DDRCOMN AH29

OCDVREFP AR8
OCDVREFN AT8

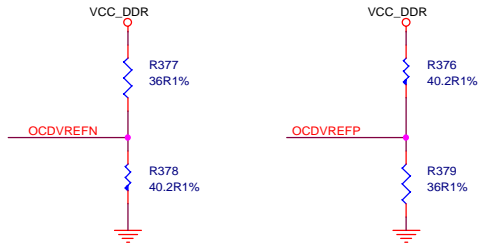
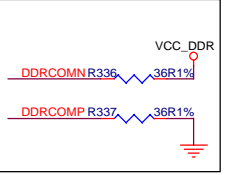
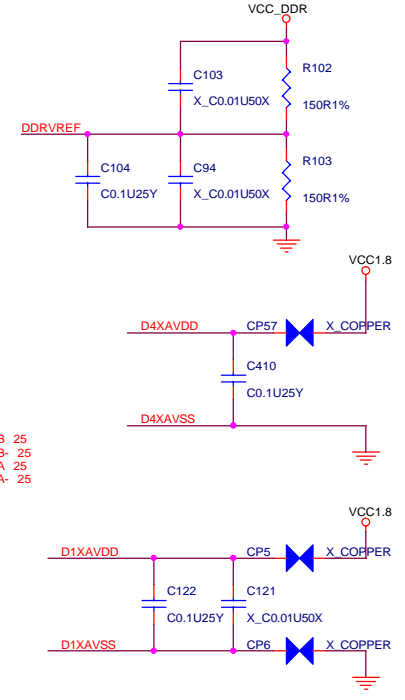
S3AUXSW# F13 S3AUXSW#

DRAM_SEL B11
When DDR2 remove
R380 external pull-up = DDR

FWSDCLKOA C399 X C10P50N
FWSDCLKOA- C398 X C10P50N
FWSDCLKOB C400 X C10P50N
FWSDCLKOB- C401 X C10P50N

22R FWSDCLKOB
22R FWSDCLKOB-
22R FWSDCLKOA
22R FWSDCLKOA-

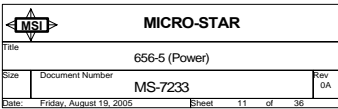
CKEA0
CKEA1
CKEA2
CKEA3

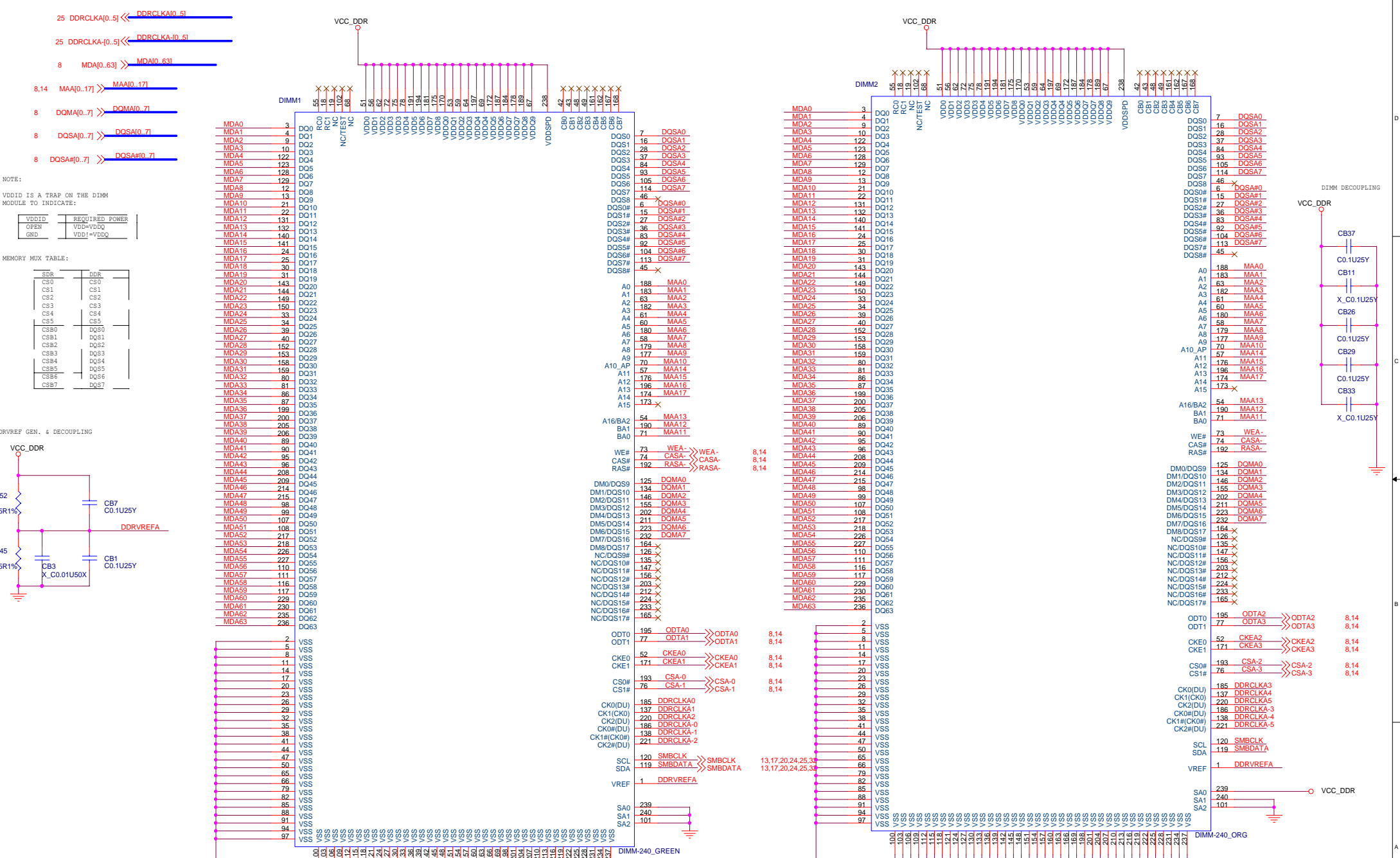


MDBI[0..63] << MDB[0..63] 13
DQMB[0..7] << DQMB[0..7] 13
DQSB[0..7] << DQSB[0..7] 13
DQSB# [0..7] << DQSB# [0..7] 13
MAB[0..17] << MAB[0..17] 13,15
CSB[0..3] << CSB[0..3] 13,15
ODTB[0..3] << ODTB[0..3] 13,15

MDB0 N29 MD0B
MDB1 M28 MD1B
MDB2 P28 MD2B
MDB3 M30 MD3B
MDB4 R28 MD4B
MDB5 M29 MD5B
MDB6 P29 MD6B
MDB7 R29 MD7B
DQMB0 N28 DQM0B
DQSB0 P30 DQS0B
DQSB#0 P30 DQS0B#
MDB8 T29 MD8B
MDB9 U29 MD9B
MDB10 W29 MD10B
MDB11 V28 MD11B
MDB12 T32 MD12B
MDB13 T30 MD13B
MDB14 V30 MD14B
MDB15 V29 MD15B
DQMB1 T28 DQM1B
DQSB1 V32 DQS1B
DQSB#1 U28 DQS1B#
MDB16 Y30 MD16B
MDB17 Y29 MD17B
MDB18 AB29 MD18B
MDB19 AC29 MD19B
MDB20 W28 MD20B
MDB21 Y32 MD21B
MDB22 AB32 MD22B
MDB23 AB30 MD23B
DQMB2 AA29 DQM2B
DQSB2 AA28 DQS2B
DQSB#2 Y28 DQS2B#
MDB24 AD32 MD24B
MDB25 AD30 MD25B
MDB26 AF30 MD26B
MDB27 AE29 MD27B
MDB28 AB28 MD28B
MDB29 AC28 MD29B
MDB30 AE28 MD30B
MDB31 AF32 MD31B
DQMB3 AD29 DQM3B
DQSB3 AD28 DQS3B
DQSB#3 AE29 DQS3B#
MDB32 AJ27 MD32B
MDB33 AM26 MD33B
MDB34 AM24 MD34B
MDB35 AK24 MD35B
MDB36 AM28 MD36B
MDB37 AK28 MD37B
MDB38 AH26 MD38B
MDB39 AH25 MD39B
DQMB4 AK26 DQM4B
DQSB4 AJ25 DQS4B
DQSB#4 AJ28 DQS4B#
MDB40 AJ19 MD40B
MDB41 AH20 MD41B
MDB42 AH18 MD42B
MDB43 AK20 MD43B
MDB44 AJ20 MD44B
MDB45 AJ18 MD45B
MDB46 AJ17 MD46B
MDB47 AH19 DQM4B
DQMB5 AH19 DQM5B
DQSB5 AK18 DQS5B
DQSB#5 AM18 DQS5B#
MDB48 AJ16 MD48B
MDB49 AJ15 MD49B
MDB50 AJ13 MD50B
MDB51 AH14 MD51B
MDB52 AM16 MD52B
MDB53 AK16 MD53B
MDB54 AK14 MD54B
MDB55 AJ14 MD55B
DQMB6 AH16 DQM6B
DQSB6 AM14 DQS6B
DQSB#6 AH15 DQS6B#
MDB56 AK12 MD56B
MDB57 AJ12 MD57B
MDB58 AN9 MD58B
MDB59 AM9 MD59B
MDB60 AH13 MD60B
MDB61 AM12 MD61B
MDB62 AM10 MD62B
MDB63 AK10 MD63B
DQMB7 AJ11 DQM7B
DQSB7 AH11 DQS7B
DQSB#7 AH12 DQS7B#

U8C
MA0B AT25 MAB0
MA1B AN25 MAB1
MA2B AM25 MAB2
MA3B AT26 MAB3
MA4B AP26 MAB4
MA5B AT27 MAB5
MA6B AM27 MAB6
MA7B AN27 MAB7
MA8B AG32 MAB8
MA9B AF24 MAB9
MA10B AT24 MAB10
MA11B AR24 MAB11
MA12B AG36 MAB12
MA13B AT28 MAB13
MA14B AG33 MAB14
MA15B AN21 MAB15
MA16B AF34 MAB16
MA17B
RASB# AT23 RASB- << RASB- 13,15
CASB# AR22 CASB- << CASB- 13,15
WEB# AT22 WEB- << WEB- 13,15
ECCD0B/CKE0B AC32 CKEB0 << CKEB0 13,15
ECCD1B/CKE1B AD36 CKEB1 << CKEB1 13,15
ECCD2B/CKE2B AF36 CKEB2 << CKEB2 13,15
ECCD3B/CKE3B AF35 CKEB3 << CKEB3 13,15
ECCD4B AC36
ECCD5B AC33
ECCD6B AE33
ECCD7B AE32
ECCDQMB AD33
ECCDQSB AE36
ECCDQSB# AD34
CS0B# AN23 CSB-0
CS1B# AM21 CSB-1
CS2B# AM23 CSB-2
CS3B# AT20 CSB-3
ODT0B AP22 ODTB0
ODT1B AR20 ODTB1
ODT2B AT21 ODTB2
ODT3B AF20 ODTB3



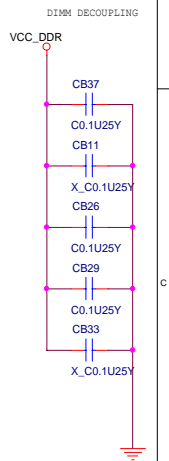
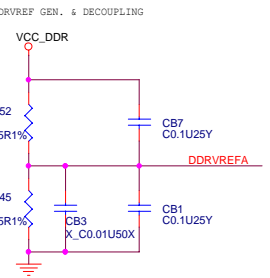


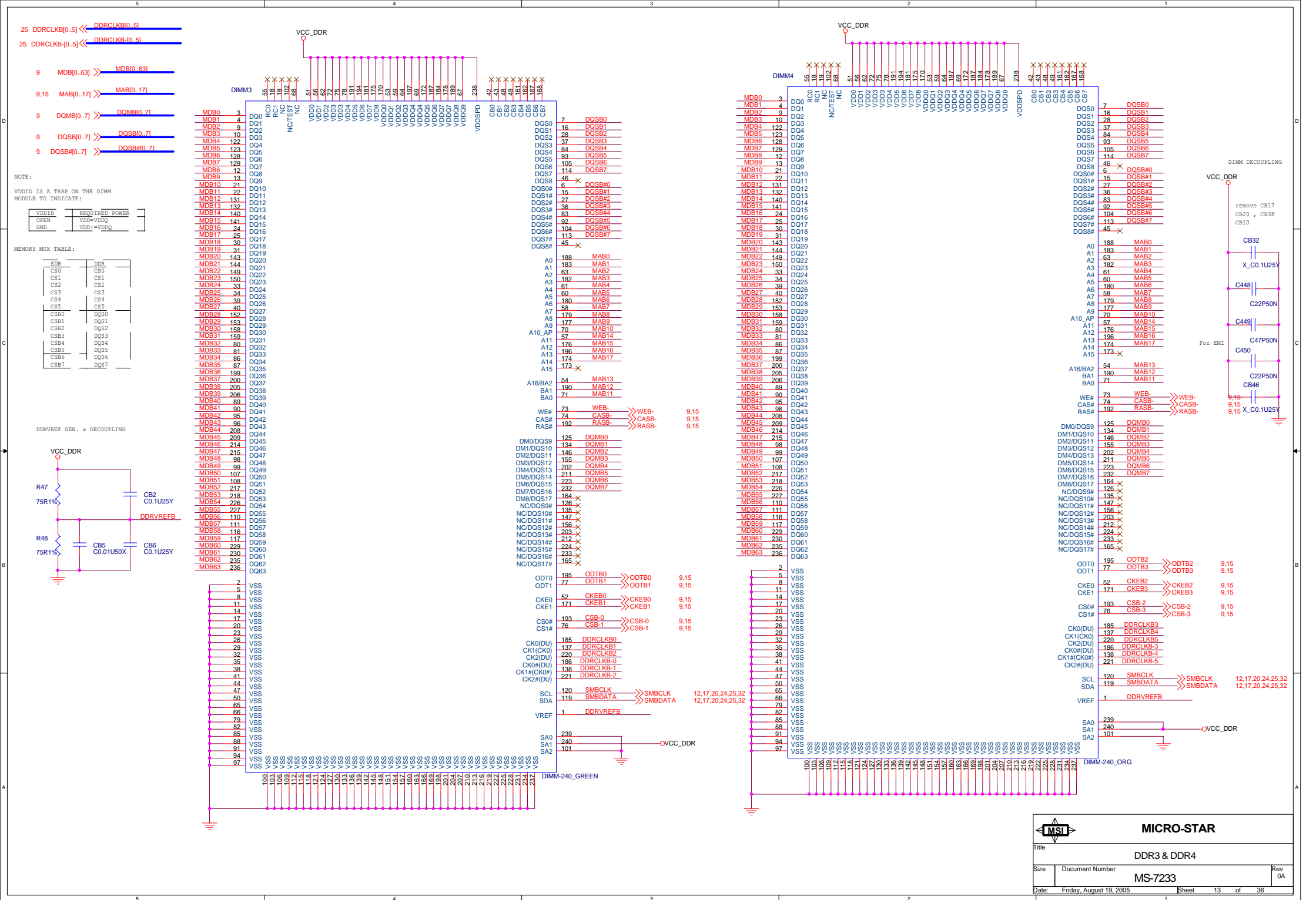
NOTE:
VDDID IS A TRAP ON THE DIMM
MODULE TO INDICATE:

VDDID	REQUIRED POWER
OPEN	VDD=VDDQ
GND	VDDI=VDDQ

MEMORY MUX TABLE:

SDR	DDR
CS0	CS0
CS1	CS1
CS2	CS2
CS3	CS3
CS4	CS4
CS5	CS5
CSB0	DQS0
CSB1	DQS1
CSB2	DQS2
CSB3	DQS3
CSB4	DQS4
CSB5	DQS5
CSB6	DQS6
CSB7	DQS7



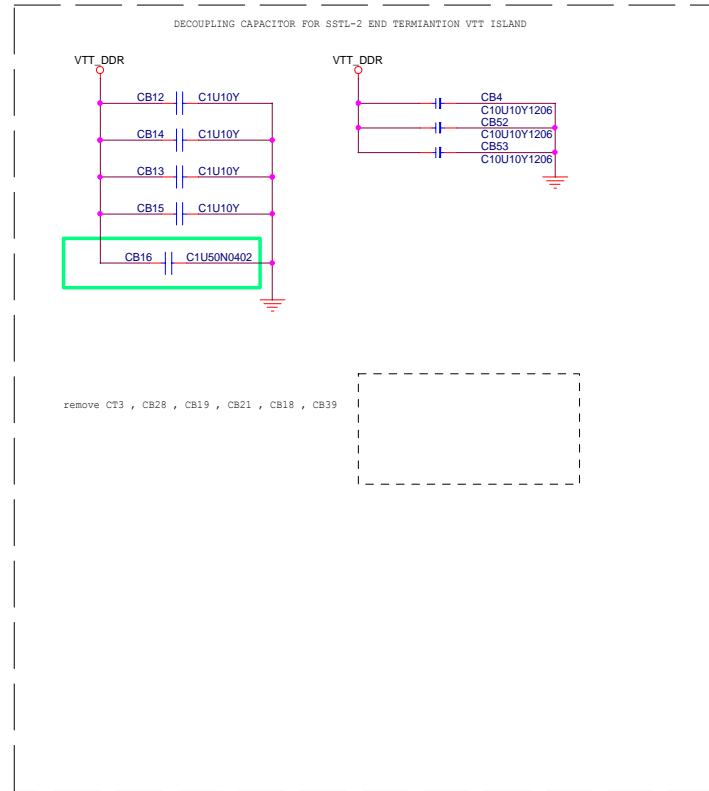
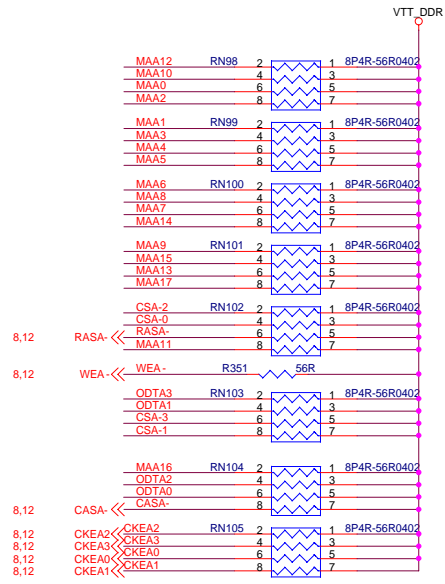


DDR TERMINATOR

SSTL-2 Termination Resistors

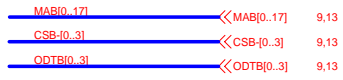


	SDR	Is	DDR	Is	Ret
MD/DQM (/DQS)	LV-CMOS	0/10/-	SSTL-2	0	B3
MA/Control	LV-CMOS	0	SSTL-2	0	B3
CS	LV-CMOS	0	SSTL-2	0	47
CKE	DD 3.3V		DD 2.5V		

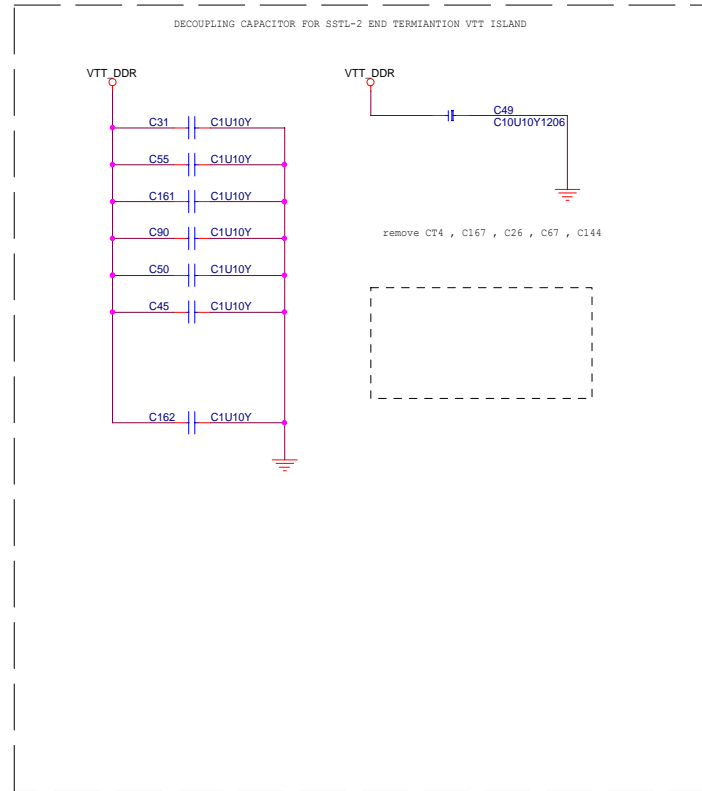
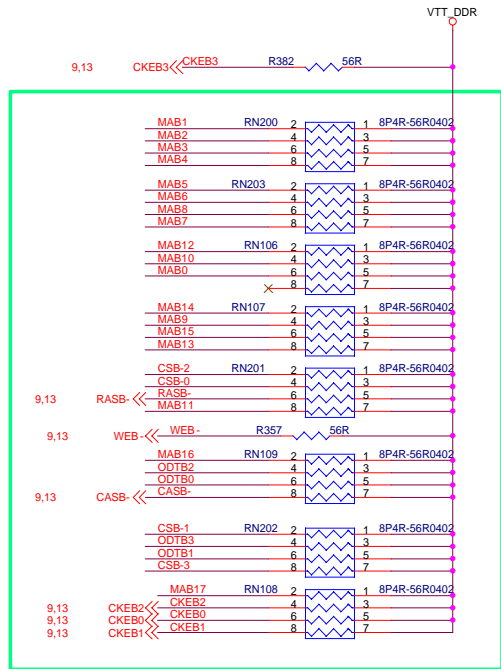


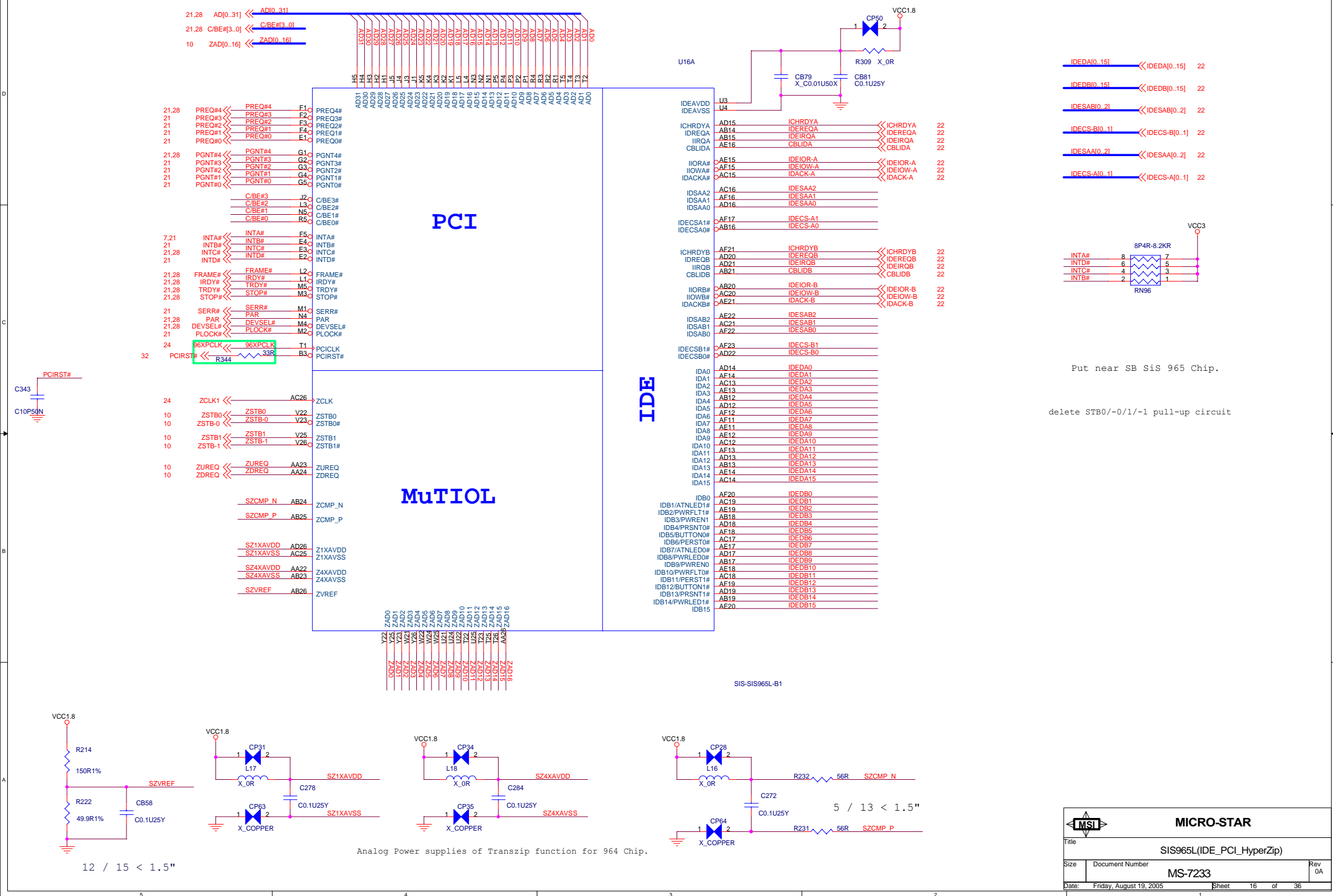
DDR TERMINATOR

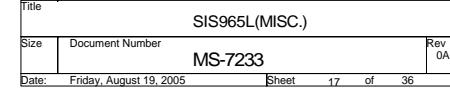
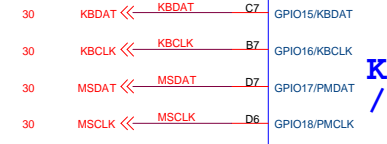
SSTL-2 Termination Resistors

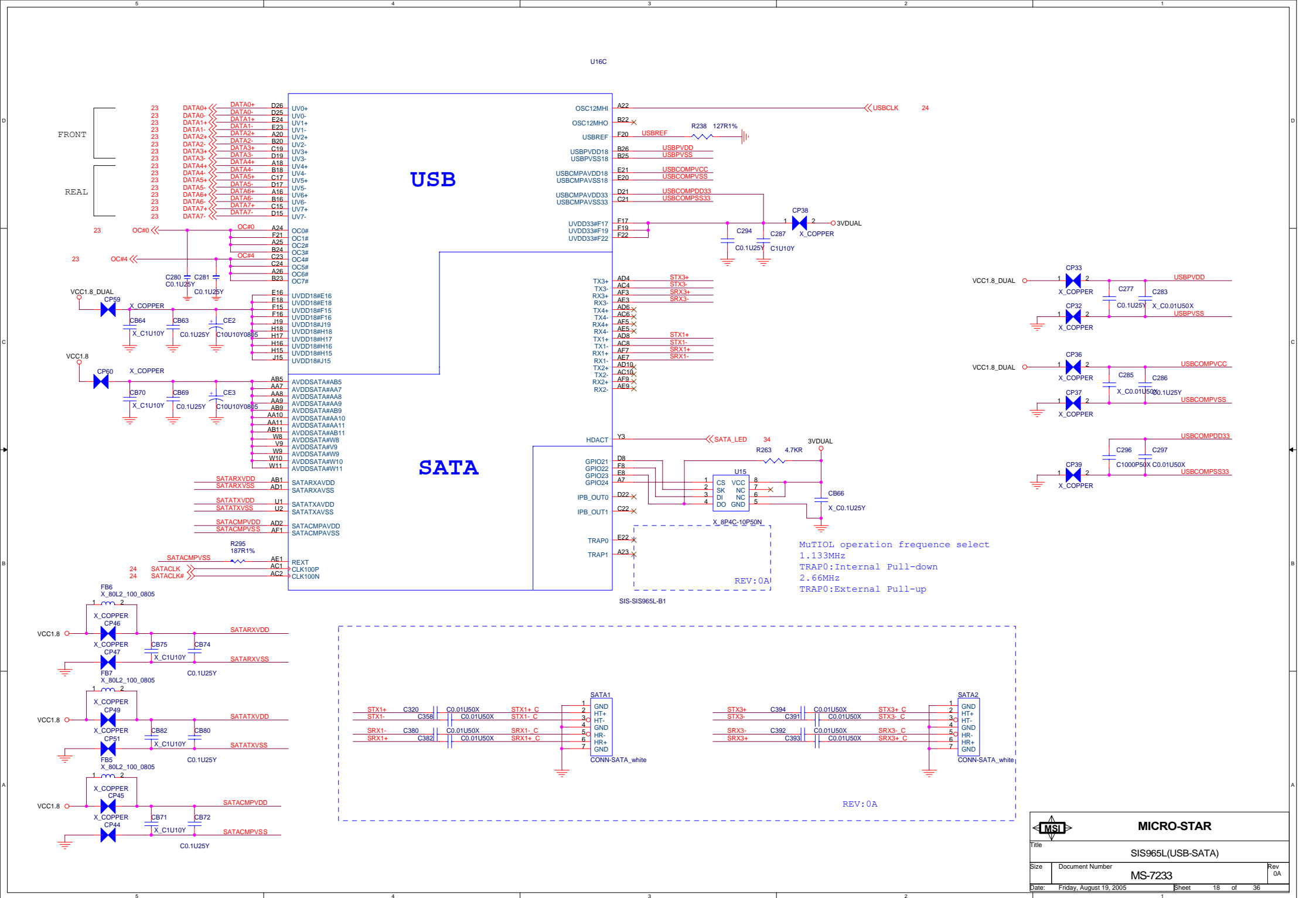


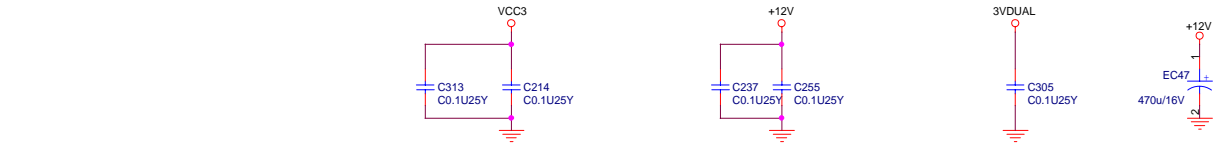
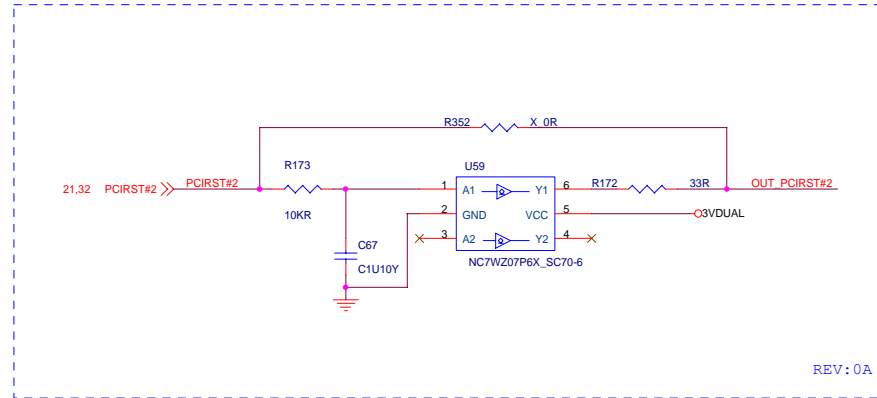
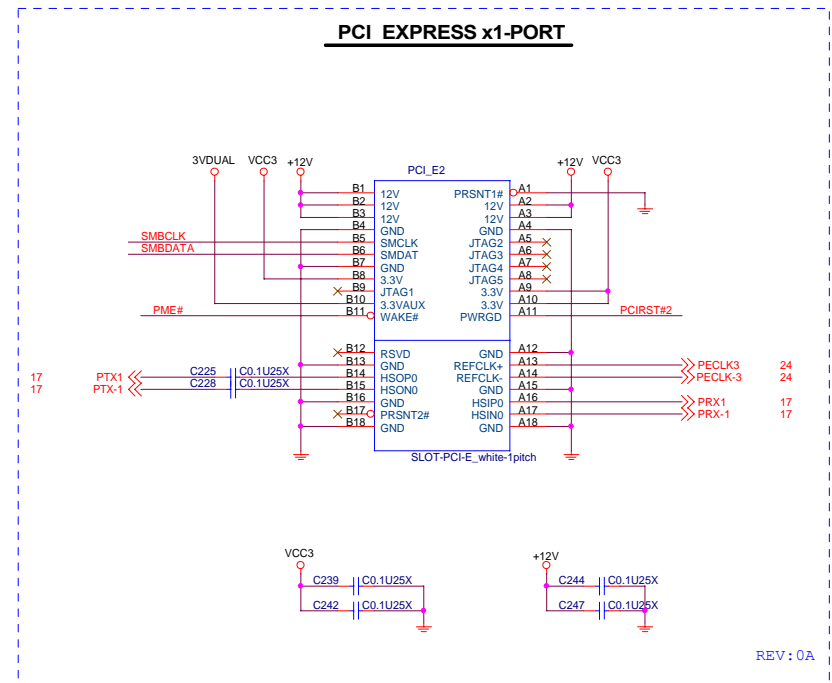
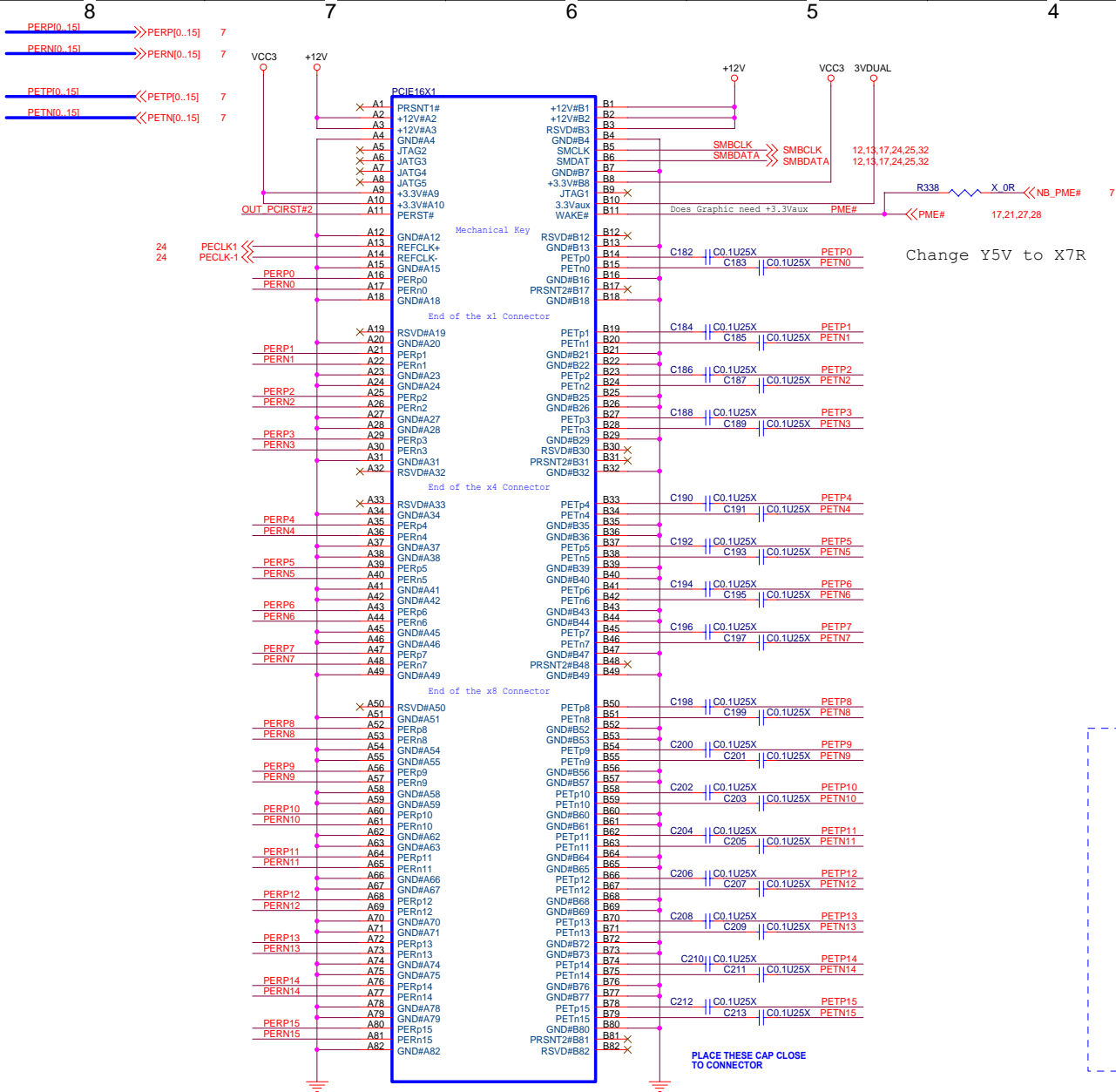
	DDR		DDR		
MD/DQM (/DQS)	LV-CMOS	R _s	SSTL-2	R _s	R _{tt}
MA/Control	LV-CMOS	0/10/-	SSTL-2	10	33
CS	LV-CMOS	10	SSTL-2	0	33
CKE	0D 3.3V	0	SSTL-2	0D 2.5V	47





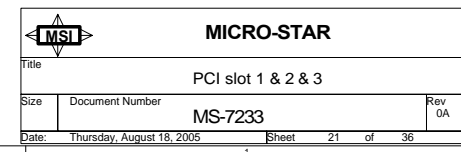
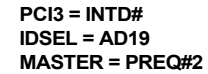




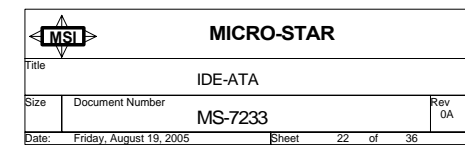


16,28 AD[0..31] << ADI[0..31]

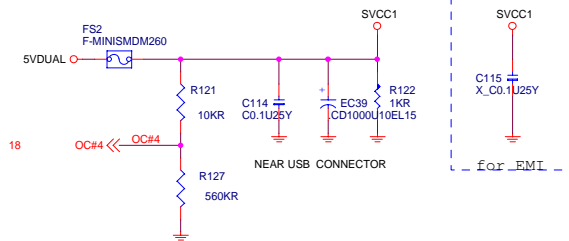
16,28 C/BE#[3..0] << C/BE#[3..0]



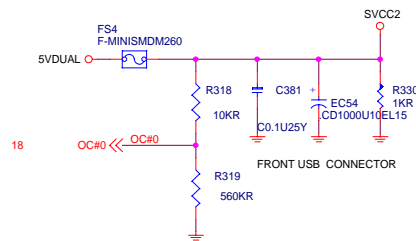
20040319
SiS AP note : A964008



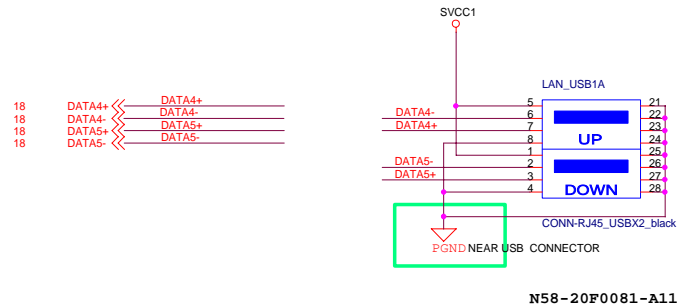
POWER CIRCUIT FOR USB PORT 4,5,6,7



POWER CIRCUIT FOR USB PORT 0,1,2,3



REAR PANEL USB CONNECTOR FOR USB PORT 4,5



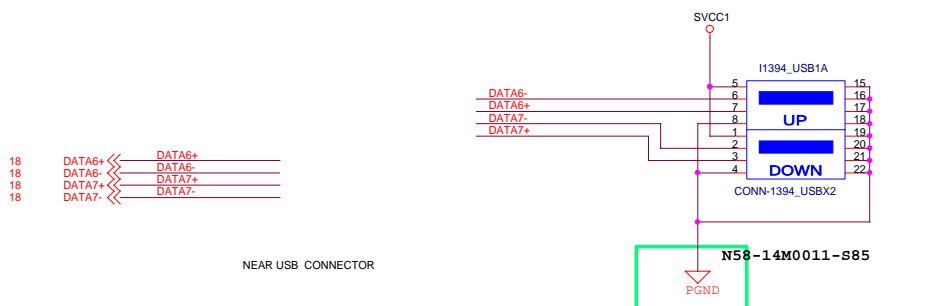
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

FRONT PANEL USB CONNECTOR FOR USB PORT 0,1



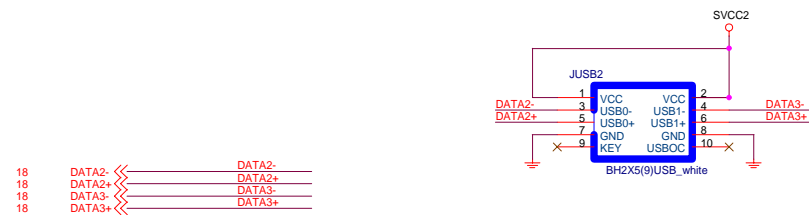
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

REAR PANEL USB CONNECTOR FOR USB PORT 6,7



22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

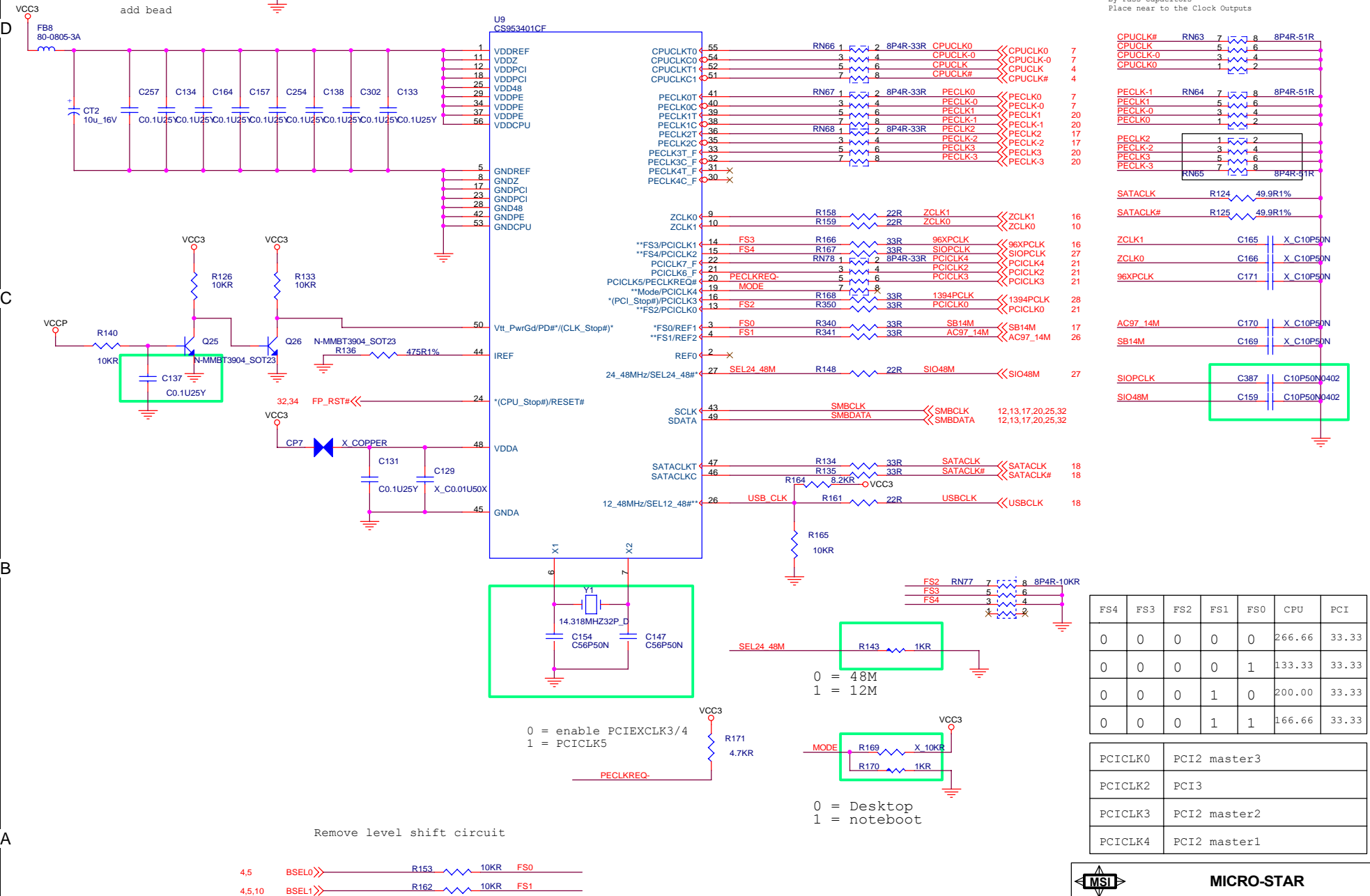
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



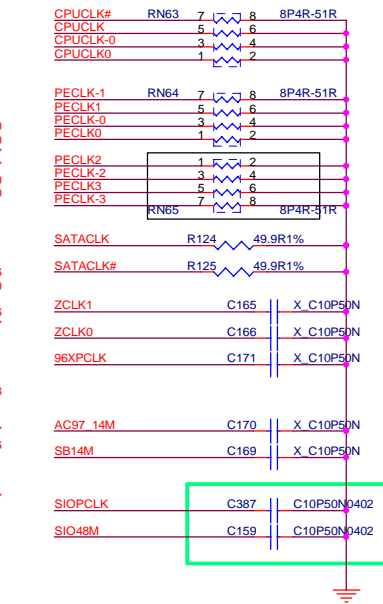
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

Main Clock Generator

OPTIONS
1. ICS953401



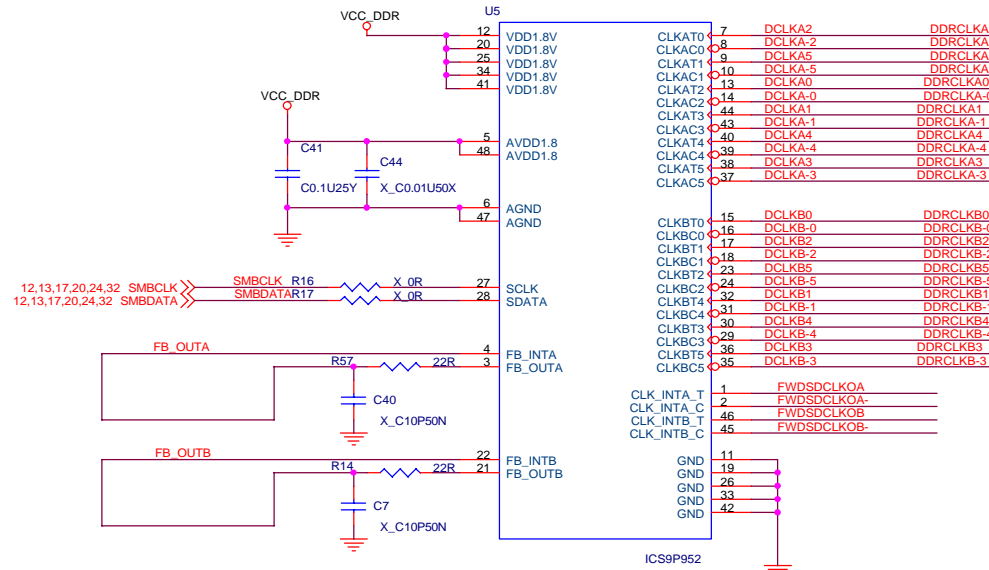
By-Pass Capacitors
Place near to the Clock Outputs



FS4	FS3	FS2	FS1	FS0	CPU	PCI
0	0	0	0	0	266.66	33.33
0	0	0	0	1	133.33	33.33
0	0	0	1	0	200.00	33.33
0	0	0	1	1	166.66	33.33

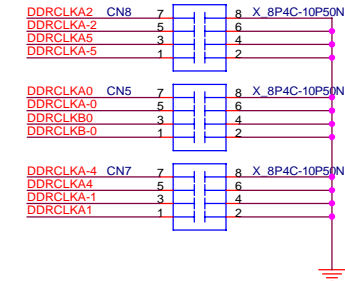
PCICLK0	PCI2 master3
PCICLK2	PCI3
PCICLK3	PCI2 master2
PCICLK4	PCI2 master1

Clock Buffer (DDR II)

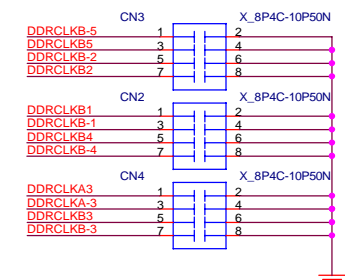


Remove damping resister

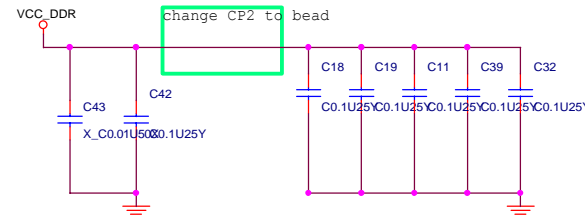
FWDSDCLKOA << FWDSDCLKOA 8
 FWDSDCLKOA- << FWDSDCLKOA- 8
 FWDSDCLKOB << FWDSDCLKOB 8
 FWDSDCLKOB- << FWDSDCLKOB- 8
 DDRCLKB[0..5] << DDRCLKB[0..5] 13
 DDRCLKB-[0..5] << DDRCLKB-[0..5] 13
 DDRCLKA[0..5] << DDRCLKA[0..5] 12
 DDRCLKA-[0..5] << DDRCLKA-[0..5] 12

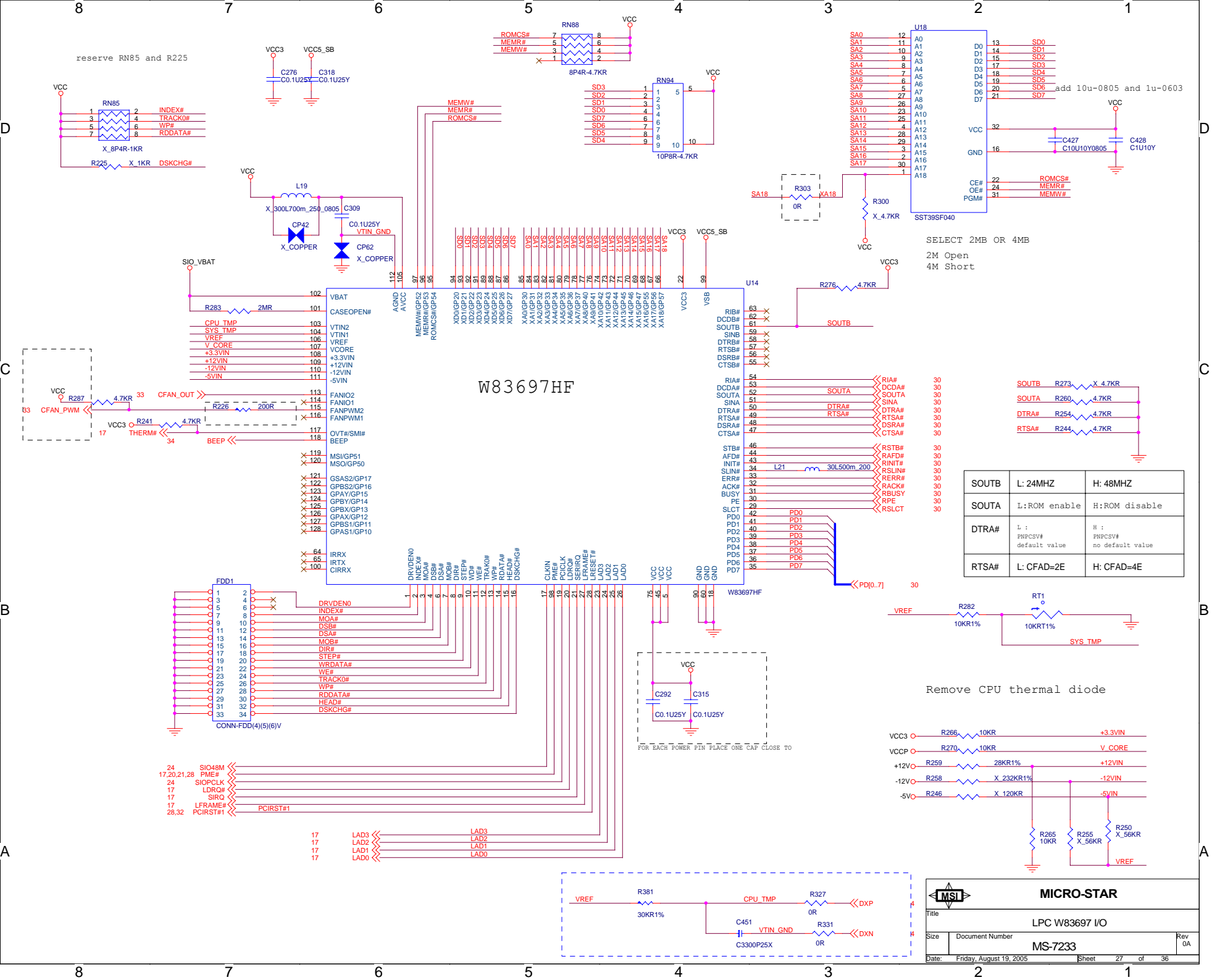


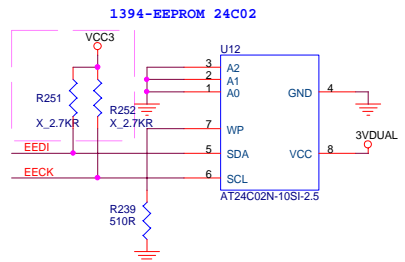
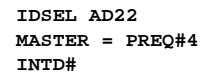
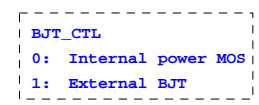
By-Pass Capacitors
Place near to the Clock Buffer



DDRVREF GEN. & DECOUPLING






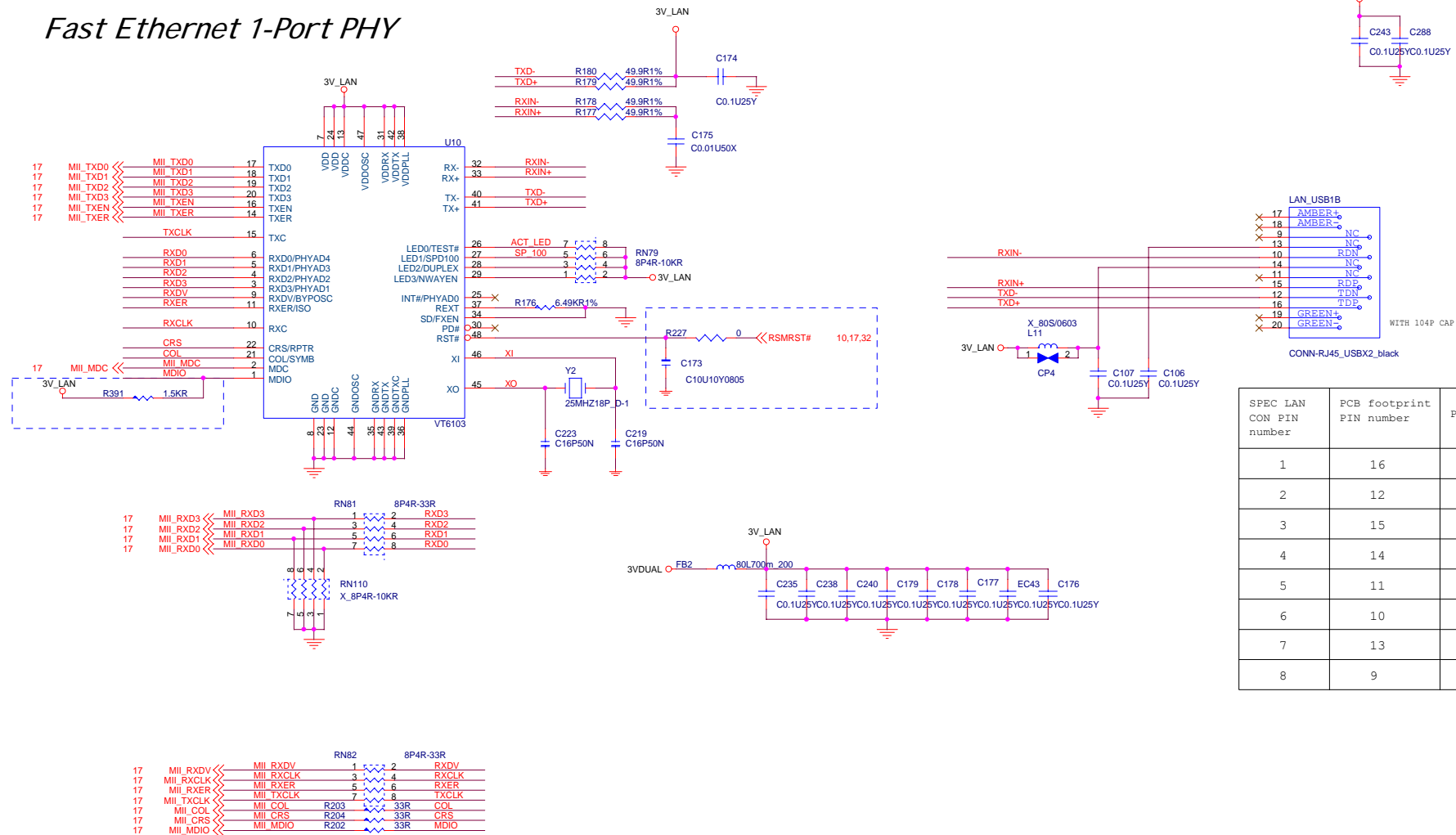
[illegible]

16,21 AD[0..31] << AD[0..31]

16,21 C/BE#[3..0] << C/BE#[3..0]

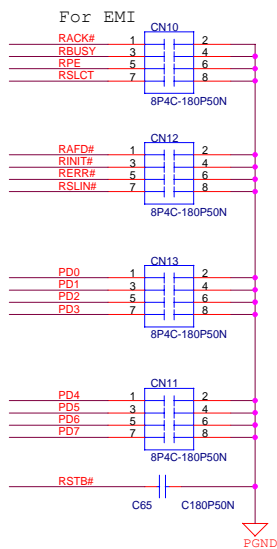
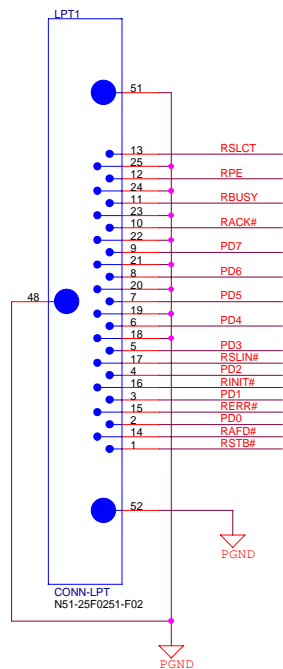
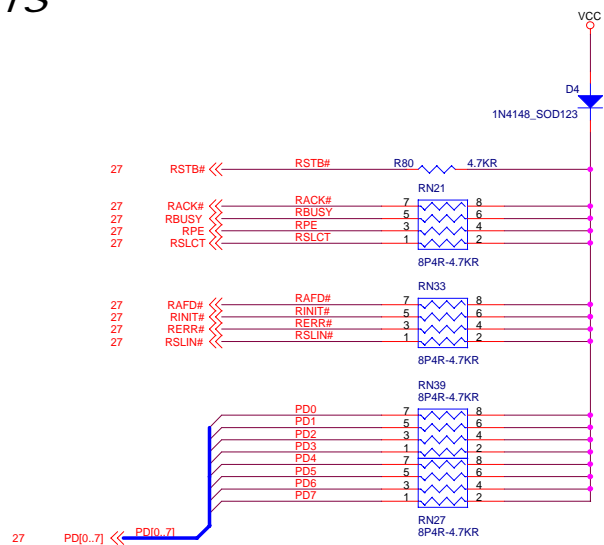
		MICRO-STAR	
Title			
1394 - VIA VT-6307			
Size	Document Number	Rev	
	MS-7233	0A	
Date:	Friday, August 19, 2005	Sheet	28 of 36

Fast Ethernet 1-Port PHY

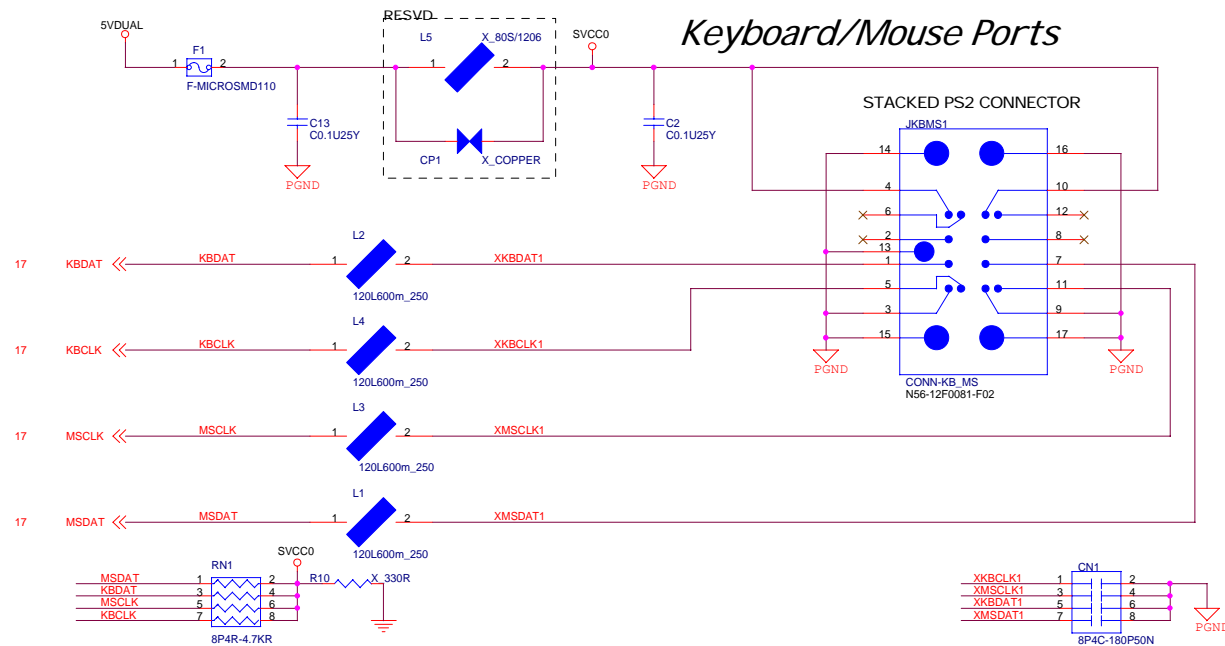


SPEC LAN CON PIN number	PCB footprint PIN number	PIN Define
1	16	TXD+
2	12	TXD-
3	15	RXIN+
4	14	TCT
5	11	NC
6	10	RXIN-
7	13	RCT
8	9	NC

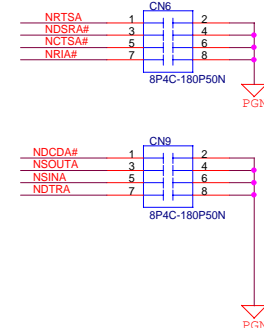
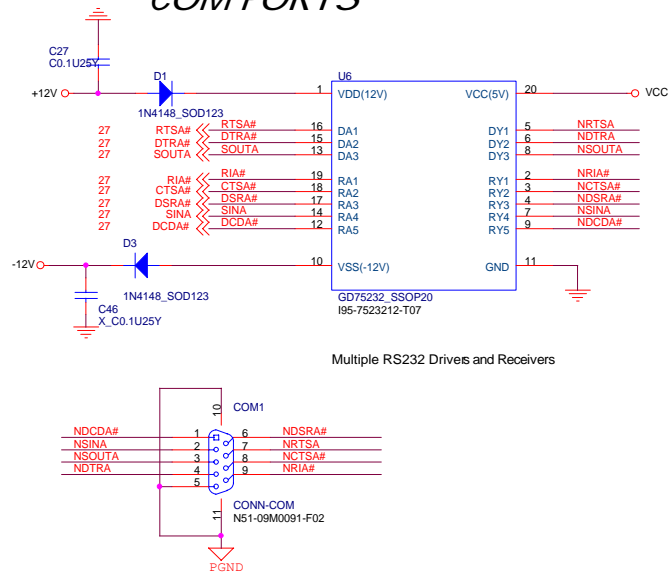
LPT PORTS



Keyboard/Mouse Ports

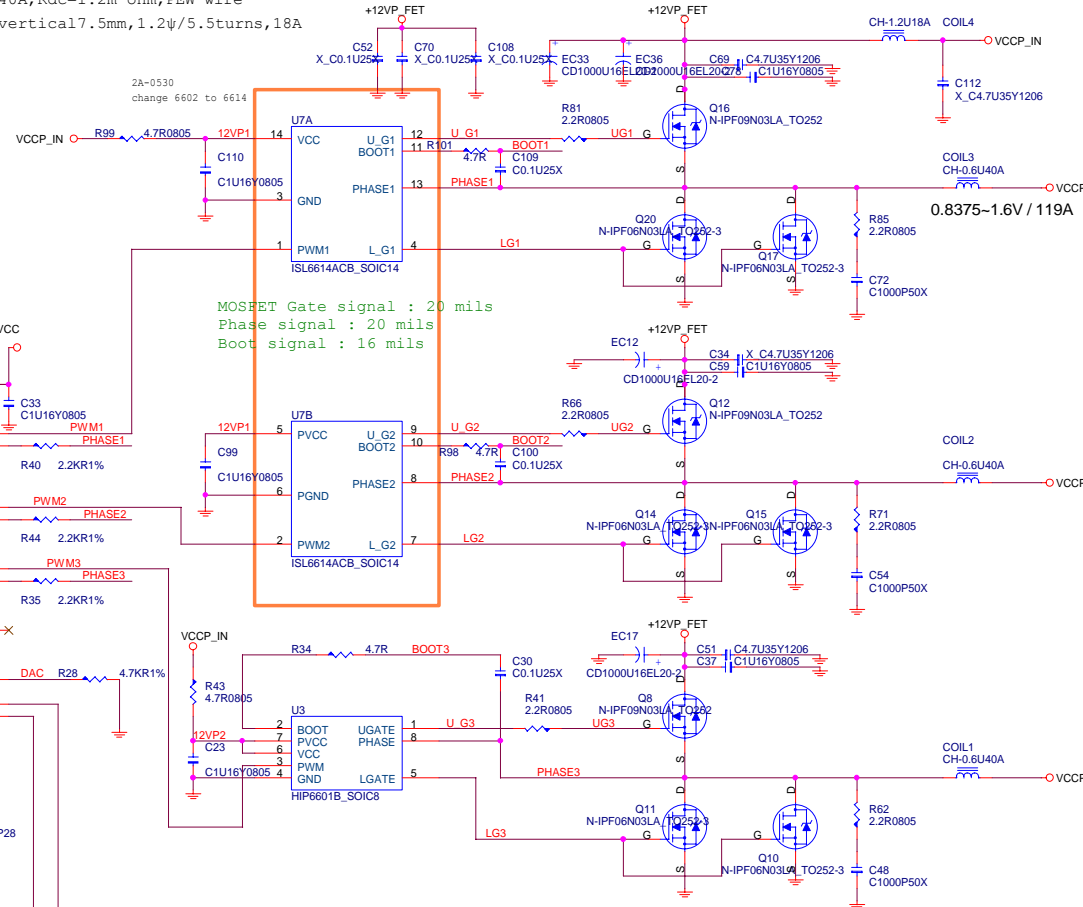


COM PORTS



MICRO-STAR		
Title LPT/COM PORT		
Size	Document Number	Rev 0A
MS-7233		
Date: Friday, August 19, 2005	Sheet	30 of 36

```
TDP = 115 W
VR_TDC = 101 A
Icc(max) = 119 A
Tejas Tcase = [P x 0.213] + 43.3
Prescott Tcase = [P x 0.25] +
43.3
```



Place these caps within socket cavity

VCCP Capacitors

EC10 1 μ F 2 560u/2.5V/8*8

EC16 1 μ F 2 560u/2.5V/8*8

EC35 1 μ F 2 560u/2.5V/8*8

EC11 1 μ F 2 680u/4V/8*9

EC13 1 μ F 2 680u/4V/8*9

EC32 1 μ F 2 680u/4V/8*9

HS-0500261-K08 HS-0500261-K08 HS-0500261-K08

VCCP

EC37
1+ (2)
.CD3300U06.3EL25

EC15
1+ (2)
.CD3300U06.3EL25

EC34
1+ (2)
.CD3300U06.3EL25

EC1
+ ()
CD1800U06.3EL20-1

EC4
+ ()
CD1800U06.3EL20-1

EC3
+ ()
CD1800U06.3EL20-1

EC2
1+ (2)
X_CD560U04OS-2

ACPI Controller

PCI 375+20+20=415mA
VCC3_SB 715mA

1.7V@250mA

Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	Standby
MEM_STR	Main	Standby	0V

1.8V STAND BY POWER

VDDPEXSB W=25mils

Pin48 pull-up 5VSB for DDR2

DDRTYPE
Pull-up 1.8V
Pull-down 2.6V

VCC VID / VID GOOD

Place MOSFET near CPU

V_FSB_VTT=

1.25V/5A

DDR VTT Power

1.25V/2.1A

5VDIMM

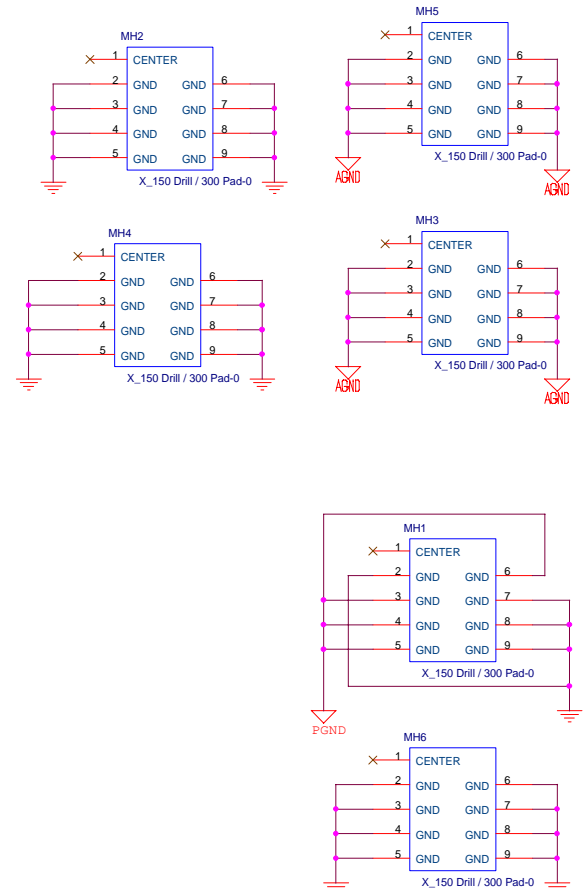
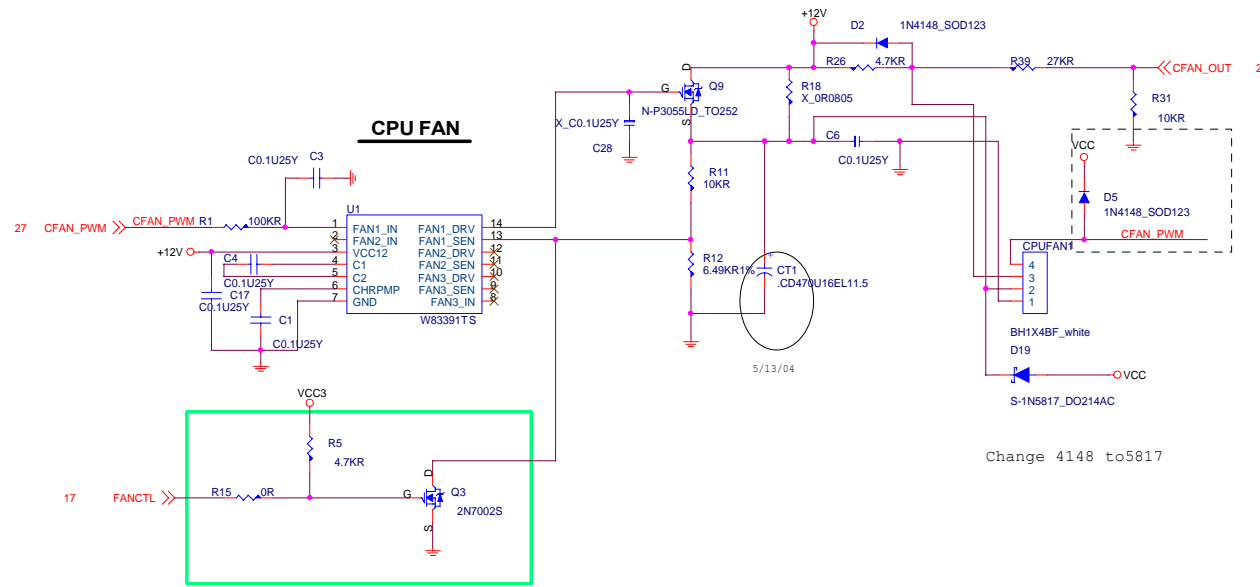
MICRO-STAR

ACPI Controller MS7

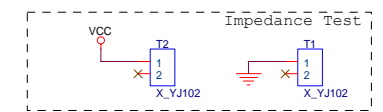
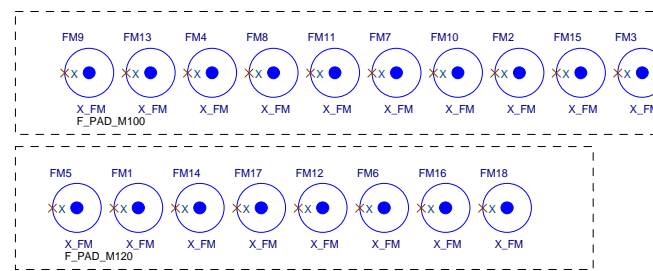
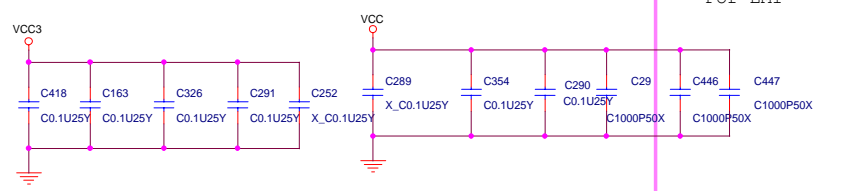
MS-7233

Title	ACPI Controller MS7	Rev	0A
Size	Document Number		
Date	Friday, August 19, 2005	Sheet	32 of 36

ATX VIA-Hole * 9

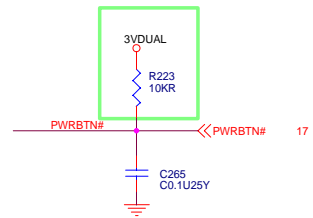
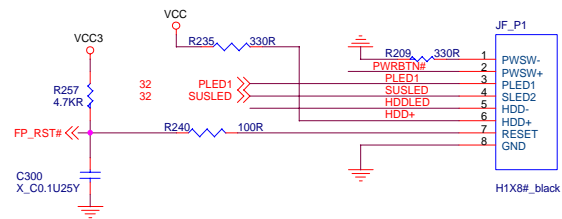


BULK / Decoupling

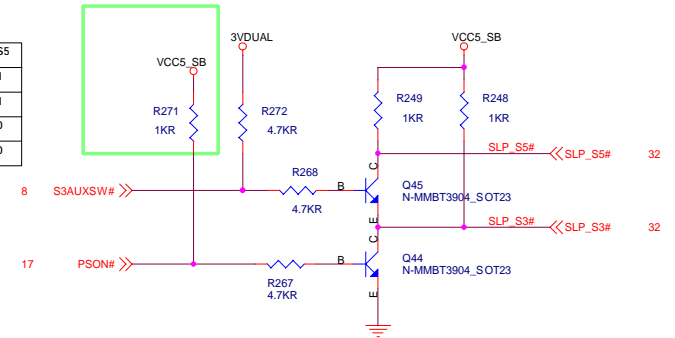


FRONT PANEL

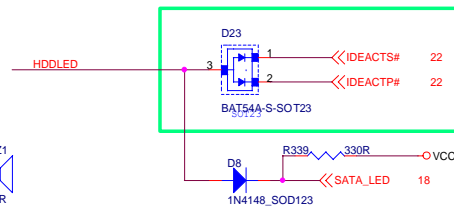
For MSI / Front Panel



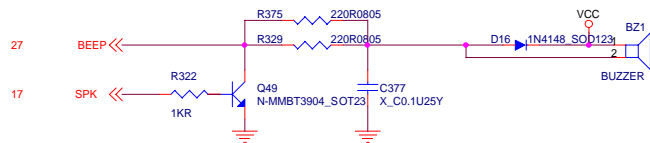
	S0	S3	S5
S3AUXSW#	1	0	1
PS0N#	0	1	1
SLP_S5#	1	1	0
SLP_S3#	1	0	0



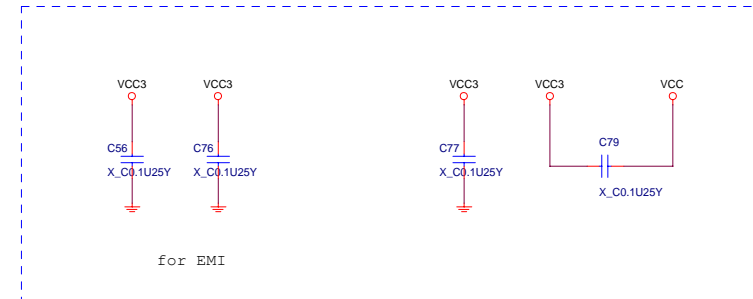
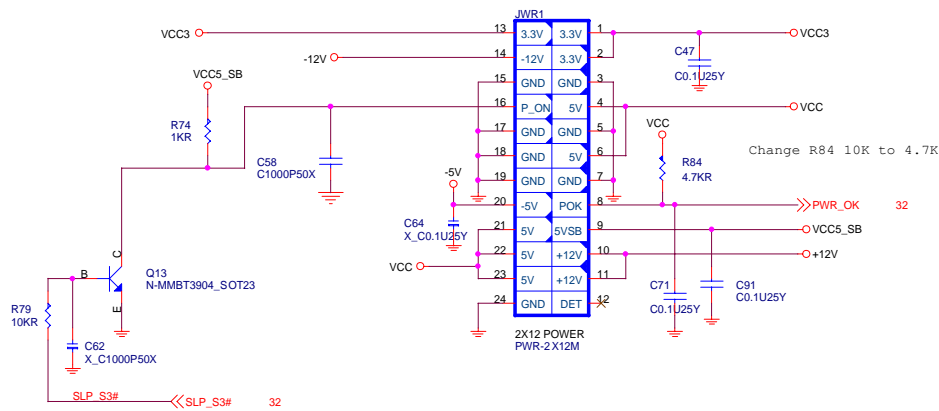
Change 8148*2 to BAT54A



Add 220R 0805



ATX Connector



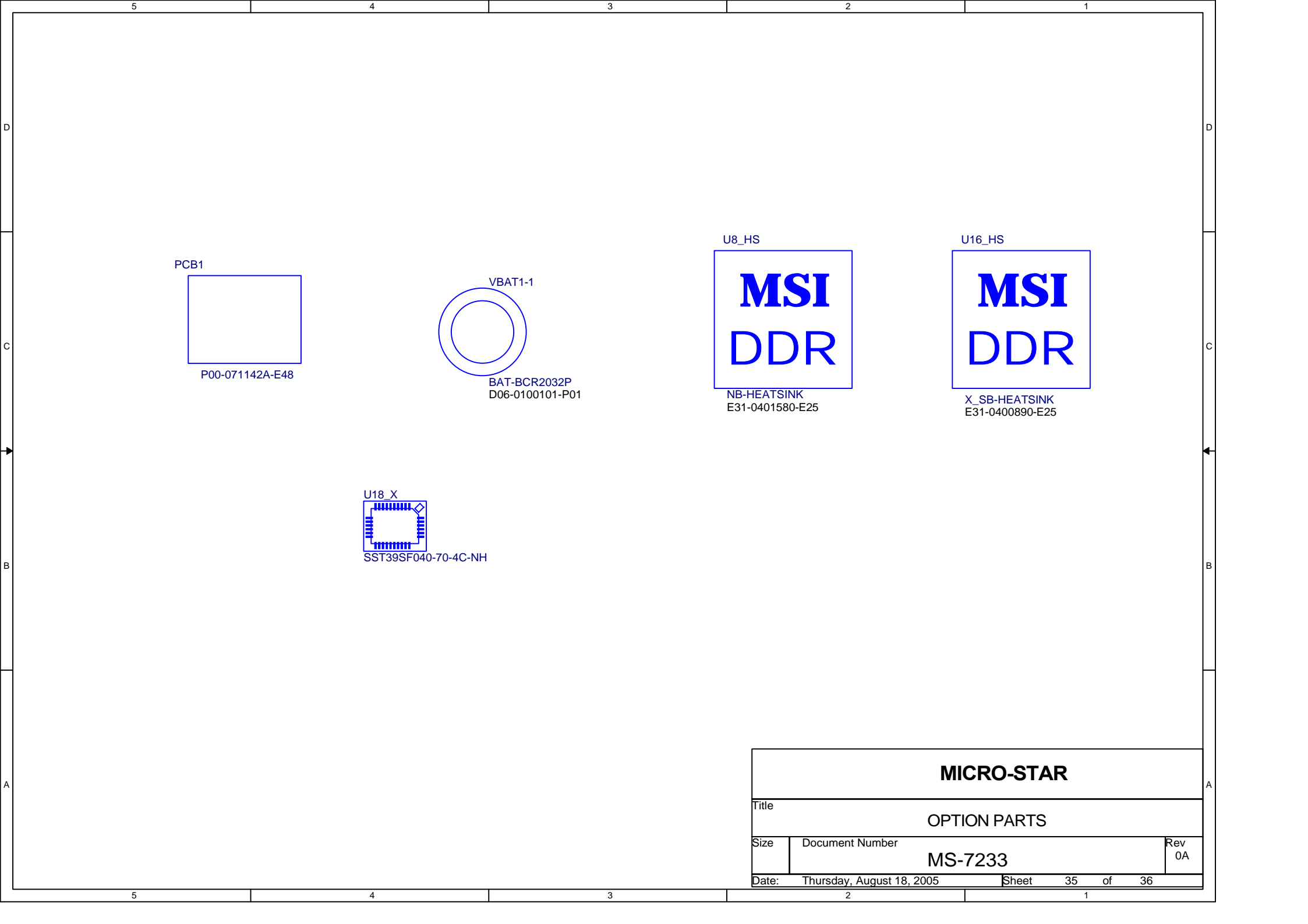
MICRO-STAR

Title FRONT PANEL

Size	Document Number
	MS-7233

Date:	Thursday, August 18, 2005	Sheet	34	of	36
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0A



PCB1
P00-071142A-E48

VBAT1-1
BAT-BCR2032P
D06-0100101-P01

U18_X
SST39SF040-70-4C-NH

U8_HS
MSI
DDR
NB-HEATSINK
E31-0401580-E25

U16_HS
MSI
DDR
X_SB-HEATSINK
E31-0400890-E25

MICRO-STAR			
Title OPTION PARTS			
Size	Document Number MS-7233		Rev 0A
Date:	Thursday, August 18, 2005	Sheet	35 of 36

MS-7114

SCHEMATIC HISTORY

Rev	Date	Page	Description
0B	2004		● Transfer from OEM3
1.00	2005/02/05	-19-	● Add bypass CAP 1u under SB solder side
		-18-	● Remove SIS964 OC#4 C419
		-24-	● Clock generator VCC3 add bead and CT2 ● Remove BSEL0,1 level shift circuit
		-25-	● Add a bead between VCC_DDR and CBVDD
		-27-	● Reserver FDD signal pull-up RN85 ● Firmware U18 power add C427 , C428
		-33-	● Change Q22 , Q24 , Q50 , Q51 type to T0263 ● Change MS7 ver:RAC to RBC and remove patch circuit ● Change VTT_DDR reference R25 , R32 to 1K
		-4-	● Remove R50 , R51 direct short
		-7-	● Change R174 to 680R , R175 to 150R
		-8-	● Add a bypass CAP C411 0.1u with DDRVREF
		-10-	● Remove VGA part
		-15-	● DDR terminator CAP all in
		-16-	● Add R344 33R for PCIRST# and remove ZSTB pull-up
		-25-	● Remove RN2 , RN3 , RN4 , RN5 , RN7 , RN8
		-26-	● Add D20 , D21 for Audio 5VSB ● Change EC58 , EC59 to 100u ● Add CN15 , CN16 , R342 , R296 , R232 , R346
		-32-	● Change C110 and C23 to 1u ● Change R8 to 1.5K ● Add EC10 , EC16 , EC35 to 560u ● Add EC11 , EC13 , EC32 to 680u
		-7-	● SIS suggest Change R109 to 10R1% , R113 to 120R1% , R90 to 261R1% R110 to 49.9R1% , R92 to 100R1% , C310 to 10p , C319 to 10p , add C117 , C119 to 103p
		-27-	● Remove -5V circuit R246 , R250
		-24-	● Change C154 , C147 to 22p

Rev	Date	Page	Description
2.00	2005/03/09		change DDR to DDR2 change CLK buffer to ICS9P952
	2005/03/23		change DDR2 slot 1/3 PN
2A	2005/05/08		change Hvref voltage with R72 R75 R92 R110 Add MS6+ VDD 5VDIMM voltage